CLAIM AMENDMENTS

Claims 1-8 (Cancelled).

9. (Currently Amended) A metal oxide semiconductor transistor comprising:

a semiconductor substrate having a surface with a device area, the device area having orthogonal longitudinal and transverse directions;

a source ~~area~~ region in the semiconductor substrate and located in the device area;

a drain ~~area~~ region in the semiconductor substrate and located in the device area;

a gate layer located on and extending across the device area, along the transverse direction of the device area, and located between the source ~~area~~ region and the drain ~~area~~ region, wherein the source and drain regions lie along a straight line extending in the longitudinal direction of the device area; and

a first control channel ~~area~~ region in the semiconductor substrate and located in the device area, between the gate layer and at least one of the source ~~area~~ region and the drain ~~area~~ region, the first control channel ~~area~~ region having a voltage threshold that gradually changes ~~in a longitudinal direction of~~ with position in the gate layer, along the transverse direction of the device area.

10. (Currently Amended) The metal oxide semiconductor transistor according to claim 9, further comprising a second control channel ~~area~~ region in the semiconductor substrate and located in the device area, between the gate layer and at least one of the source ~~area~~ region and the drain ~~area~~ region so that the first and second control channel regions are located on opposite sides of the gate layer, wherein the first and second control channel ~~area between the gate layer and at least one of the source area and the drain area has a~~ regions have respective voltage ~~threshold~~ thresholds that gradually ~~increases~~ change with position, in opposite directions, along the ~~longitudinal~~ transverse direction~~, and the second channel area has a voltage threshold that gradually decreases in the longitudinal direction~~ of the device area.

11. (Currently Amended) The metal oxide semiconductor transistor according to claim 9, wherein the first control channel ~~area~~ region includes a channel diffusion ~~area~~ region that has an impurity concentration that gradually changes ~~in~~ along the ~~longitudinal~~ transverse direction of the device area.

12. (Currently Amended) The metal oxide semiconductor transistor according to claim 9, further comprising an insulating layer located on the first control channel ~~area~~ region, the insulating layer having a thickness that gradually changes ~~in~~ along the ~~longitudinal~~ transverse direction of the device area.

13. (New) The metal oxide semiconductor transistor according to claim 9, further comprising a second control channel region in the semiconductor substrate and located in the device area, between the gate layer and at least one of the source region and the drain region so that the first and second control channel regions are located on opposite sides of the gate layer, wherein the first and second control channel regions have respective voltage thresholds that gradually change with position, in the same direction, along the transverse direction of the device area.

14. (New) A metal oxide semiconductor transistor comprising:

a semiconductor substrate having a surface with a device area, the device area having orthogonal longitudinal and transverse directions;

a source region in the semiconductor substrate and located in the device area ;

a drain region in the semiconductor substrate and located in the device area;

a gate layer located on and extending across the device area along the transverse direction of the device area and located between the source region and the drain region, wherein the source and drain regions lie along a straight line extending in the longitudinal direction of the device area, and the gate layer covers a gate area of the device area;

a control gate layer covering a control gate area of the device area, the control gate layer having a first part extending across only part of the device area in the transverse direction of the device area and including a first end, and a second part extending across only part of the device area along the transverse direction of the device area and having a second end, the first part being located in the device area between the gate layer and at least one of the source region and the drain region with a first gap, along the transverse direction of the device area, between the first end and a boundary of the device area extending along the longitudinal direction of the device area; and

a diffusion region in the semiconductor substrate and located in the device area, between the gate area and the control gate area.

15. (New) The metal oxide semiconductor transistor according to claim 14, wherein the gate layer and the control gate layer are located in a common plane.

16. (New) The metal oxide semiconductor transistor according to claim 14, wherein a portion of the second part of the control gate layer is disposed outside the device area.

17. (New) The metal oxide semiconductor transistor according to claim 14, wherein the second part of the control gate layer is located on the device area, between the gate layer and one of the drain region and the source region so that the first and second parts of the control gate layer are located on opposite sides of the gate layer, and including a second gap along the transverse direction of the device area between the second end of the second part of the control gate layer and the boundary of the device area.

18. (New) The metal oxide semiconductor transistor according to claim 14, wherein

the gate layer has, outside the device area, a first contact area connected to a first electrode,

the gate control layer has, outside the device area, a second contact area connected to a second electrode, and

the first contact area and the second contact area are disposed on the same side of the device area.

19. (New) The metal oxide semiconductor transistor according to claim 14, wherein

the gate layer has, outside the device area, a first contact area connected to a first electrode,

the gate control layer has, outside the device area, a second contact area connected to a second electrode, and

the first contact area is on an opposite side of the device area from the second contact area.

20. (New) The metal oxide semiconductor transistor according to claim 14, wherein

the first and second parts of the control gate layer are located on the device area between the source region and the gate layer,

the second end and the first end are located opposite each other and separated by a second gap, and

the control gate layer has a third part connecting the first part to the second part, at least part of the third part being located outside the device area.

21. (New) The metal oxide semiconductor transistor according to claim 14, wherein the diffusion region has the same conductivity type as the source region and the drain region, and an impurity concentration lower than impurity concentrations in the source region and the drain region.